Efficiency Improvement Techniques at Low Power Levels for Linear CDMA and WCDMA Power Amplifiers (Invited Paper)

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Abstract – **Power amplifiers are significant contributors to current consumption within mobile phones resulting in continued focus on design techniques to improve power amplifier efficiency. The techniques presented here use variable bias current and supply voltage, which allow enhanced efficiency at low power levels, and variable load impedance, which provides tradeoffs for optimum linearity and efficiency as a function of power level and battery voltage.**

I. Introduction

The goal of increasing mobile phone standby and talk-time between battery charges is continually being driven by customer desire and stiff competition. The rate of current consumption from the battery is directly related to the amount of time during which phone operation can be maintained between battery charges. Mobile phone power amplifiers draw significant battery current, and although improvements in battery technology continue to be made, there is still significant focus on improved power amplifier design techniques.

Power amplifiers for CDMA and WCDMA handset applications must be designed and manufactured to meet certain maximum output power specifications (i.e. Linearity and Power Added Efficiency at 28dBm for typical CDMA IS-95 standard). This is accomplished by optimizing the bias point and load line at maximum output power and minimum supply voltage, but at the expense of high current consumption at low output power levels.

Published data from CDG (CDMA Development Group) testing in urban and suburban environments have been helpful in understanding the relationship between the probability distribution function (pdf) and the power amplifier output for a typical CDMA mobile phone (Figure 1). From these data, the percentage of time that a power amplifier operates at backed off power levels is shown to be significant, therefore, design techniques that improve the efficiency at low power and at the same time allow full specification compliance at high power are useful for lowering the expected or average current consumption.

Power, P, is a random variable, so the expected or average current, $\langle I_C \rangle$, can be determined by integrating the product of the pdf of the power, $f(P)$, and the power amplifier current as a function of power, $I_C(P)$, as shown in equation 1. In the analysis of power amplifier data presented in this paper, discrete urban and suburban probabilities of the random variable power, $p(P_i)$, were used along with measured current consumption recorded at discrete power levels, $I_C(P_i)$, to calculate the expected or average current consumption (equation 2), where P_i represents the i^{th} power level.

$$\langle I_C \rangle = \int_{P\min}^{P\max} I_C(P) \cdot f(P) \cdot dP \qquad (1)$$

$$\langle I_C \rangle = \sum_{i=1}^{M} p(P_i) \cdot I_C(P_i) \qquad (2)$$

Increasing power amplifier efficiency at low power levels can be achieved by reducing excess current and by increasing the signal voltage relative to the supply voltage. These results are achievable by direct control of the power amplifier quiescent current, supply voltage, and/or load.

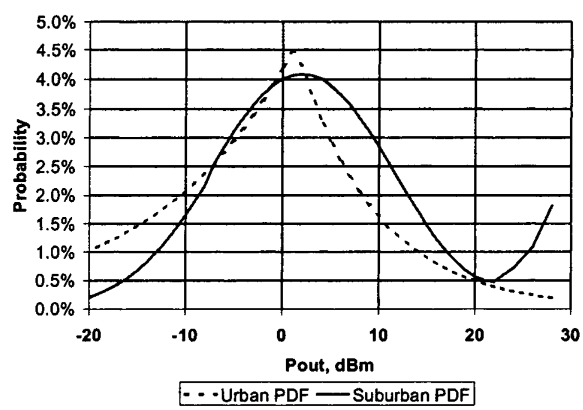

Fig. 1. Power amplifier probability density function for IS-95 urban and suburban environments (5dB offset for worst case PCS losses between PA and antenna).

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II. Variable Bias Point Selection

Variable Bias Point Selection techniques take advantage of the ability of the power amplifier to meet linearity requirements at low power levels with quiescent current and supply voltage significantly lower than required for maximum power operation.

A. Variable Quiescent Current Selection

Several methods have been demonstrated to realize variable quiescent current. The simplest is direct control by a digital voltage applied from the mobile phone system. This technique can be expanded to include two or more bias control inputs in order to achieve multiple quiescent current levels.

In the example of a Conexant System Smart™ PA, two digital control pins are used to modify the bias conditions for a two-stage power amplifier. The control logic is designed to be switched at various power thresholds, to achieve current reduction at low output power conditions. Consequently, the power amplifier can operate in up to four power modes. When operating at the highest quiescent current mode, the System Smart™ PA functions like a regular power amplifier with quiescent current near 100mA for nominal conditions. The quiescent current can be reduced to as low as 33mA at lowest quiescent current mode resulting in improved power-added efficiency. Figure 2 shows a typical battery current consumption with respect to power output for a cellular band System Smart™ power amplifier designed to operate in three power ranges.

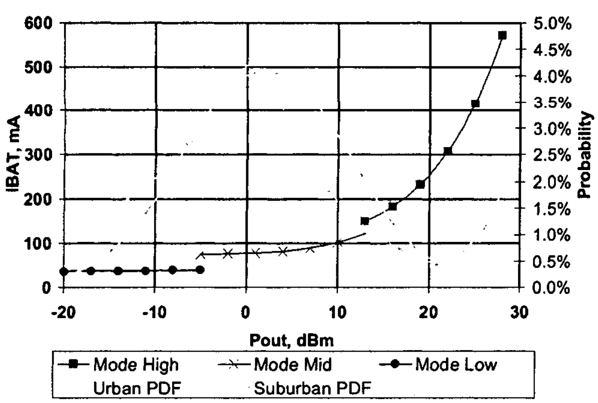

Fig. 2. Typical battery current consumption with respect to power for output of a cellular band System Smart™ PA.

It should be noted that the approach of selectable quiescent current bias states renders a simple and cost-effective solution to achieve a 20 to 30 percent reduction in average current consumption. Moreover, the implementation can be accomplished on the GaAs RFIC level, casting virtually no impact on package form factor. Furthermore, the introduction of low/medium-mode bias states for saving current is not made at the expense of performance degradation in high mode.

Increased flexibility can be implemented for quiescent current selection by incorporating the bias point selection functions into a separate CMOS integrated circuit. This approach supports options for digital/analog control, eliminates the requirement for a regulated reference voltage and provides excellent bias insensitivity to temperature variation by capitalizing on the versatility offered by mature CMOS circuit techniques and technology. Other desired features such as power detection and advanced bias techniques can also be integrated on CMOS. Naturally, all of these extra functions are obtained at the expense of form factor and cost.

An example of CMOS assisted PA bias has been realized in a Conexant WCDMA power amplifier. Figure 3 shows the dependence of the linear output power (maximum Pout at which the linearity criterion ACPR(5MHz) = –39dBc is met) and the corresponding total current (Ic) on the bias control voltage (Vctrl) for a WCDMA power amplifier. Vctrl controls the quiescent current of the amplifier.

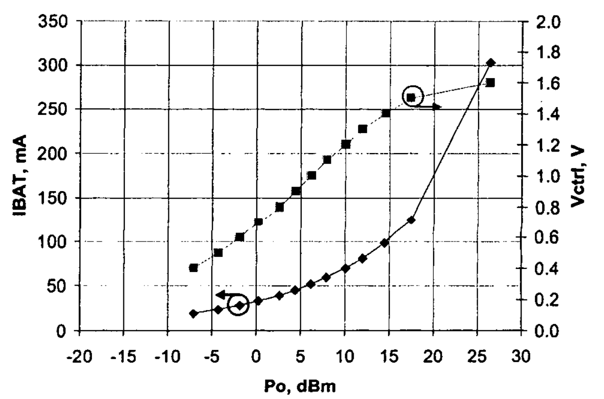

Fig. 3. Smart Bias control for a 26dBm WCDMA PA operating at 1950MHz, Vcc=3.4V.

Depending on the transmitter power level, an optimum quiescent current can be selected as suggested by Figure 3. The discontinuities observed here (e.g. at Vctrl=1.5V) are caused by the large gain expansion observed in power amplifiers biased at low quiescent currents. The maximum linear Pout level can be continuously adjusted through Vctrl in two ranges: (a) a low power range (e.g. Pout<17dBm) and (b) a high power range (e.g. Pout>25dBm). The controllability of the maximum Pout in the lower range is very sensitive to Vctrl. As a result, the current can be minimized through proper Vctrl (i.e. quiescent current) for an arbitrary Pout level of operation. For example, if the PA needs to transmit Pout=0dBm, an optimum bias level of Vctrl=0.7 V (quiescent current=27mA) can be selected. This results in a minimum current dissipation of Icc=35mA at this RF drive level.

B. Variable Operating Voltage Selection

Power amplifier efficiency, η, is a strong function of the ratio of peak RF output voltage (V_O) to DC voltage supplied to the power amplifier (V_{PA}). Equation 3 shows the simple relationship for a Class A power amplifier, but similar relationships exist for other classes of power amplifier such as Class AB.

$$\eta = \frac{(V_O / V_{PA})^2}{2} \tag{3}$$

Since the loadline must be tuned for operation at rated power, at low power levels the peak RF output voltage is low compared to the supply voltage. For this reason, the efficiency will also be low. By reducing the voltage supplied to the power amplifier (V_{PA}), as a function of output power, very high efficiencies can be achieved over the transmitter dynamic range. As the required PA power level increases, V_{PA} can be increased in order to meet key system linearity compliance [for example, adjacent channel power ratios (ACPR)].

Equation 4 illustrates why, at rated power, linearity decreases as a function of decreased V_{PA}. As the supply voltage decreases the saturated transmitter power (P_{MAX}) decreases. AM-to-AM distortion results due to clipping of the voltage waveform. $V_{PA\text{-}MIN}$ represents the minimum voltage from the battery as seen at the power amplifier, V_{SAT} represents the saturation voltage of the power amplifier transistor, and R_{LOAD} represents the load impedance as seen by the output of the power amplifier final transistor.

$$P_{MAX} \approx \frac{(V_{PA\text{-}MIN} - V_{SAT})^2}{2 \times R_{LOAD}} \tag{4}$$

In order to practically implement the Variable Operating Voltage technique, a Buck-type configured DC-to-DC converter can be used, where the output voltage to the PA (V_{PA}) is less than or equal to the battery or supply voltage (V_{BAT}). This has been demonstrated using a Power Management Integrated Circuit (PMIC). In addition to an increase in power amplifier efficiency (Eff), the DC-to-DC conversion significantly reduces battery current (I_{BAT}) by Equation 5, where I_{PA} is the power amplifier current.

$$I_{BAT} = I_{PA} \cdot \frac{V_{PA}}{V_{BAT}} \cdot \frac{1}{Eff} \tag{5}$$

A cellular CDMA Power Amplifier utilizing *Variable Operating Voltage Selection* has been characterized. The quiescent current as seen by the battery reduced from 100mA to 20mA as the supply voltage reduced to as low as 0.8V. Linearity was maintained for output powers less than 10dBm at full battery charge (4.2V). Figure 4 shows the resulting battery current consumption.

In this example, the conversion efficiency of the DC-to-DC converter is assumed to be 100%. A practical DC-to-DC converter, however, operates at between 75% and 85% efficiency at the highest current. This is not of major concern, because at lower power levels (i.e. lower I_{PA} levels) representing the highest probability of occurrence, the DC-to-DC conversion loss represents very little efficiency loss, and the average efficiency is not significantly affected.

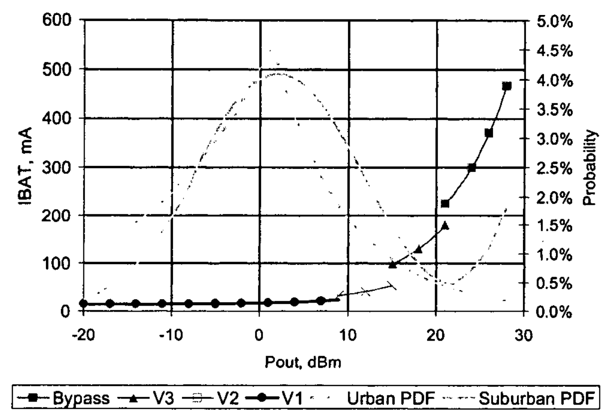

Fig. 4. Typical battery current with respect to power for output of a cellular band PA controlled by a variable operating voltage PMIC.

With this technique, we see a substantial average current reduction of between 60 and 75 percent for a given operating voltage. This technique brings the added benefit of greater reliability and lower thermal rise in the handset package. Ultimately, the dynamic operating voltage system can improve talk time, with minimal increase in cost and board area for the PA sub system. This can be accomplished by integrating the Buck converter function into the system's PMIC.

TABLE I

SUMMARY OF LOW POWER EFFICIENCY ENHANCEMENT TECHNIQUES

PA Configuration	Average Current		Percent Reduction		PA Complexity	System Considerations
	Urban	Suburban	Urban	Suburban		
Standard	116.2	139.1	0.0%	0.0%	Low	None
Smart	76.4	108.2	34.3%	22.2%	Low / Medium	Switching Control
Load Switched	46.2	76.7	60.2%	44.9%	High	Switching Control
PMIC	28.3	49.8	75.6%	64.2%	Low	PMIC Design

III. VARIABLE LOAD IMPEDANCE

A different approach can be taken to increase the ratio of the square of peak RF output voltage (V_O) to the square of DC battery voltage (V_{BAT}). Since for a given power level, V_O will increase proportionally to the square root of the load impedance, load switching can also be employed to enhance low power efficiency. At low power levels the load is switched to a higher impedance. This results in an increase in V_O resulting in higher efficiencies. At the same time, although the increase in load impedance (R) results in a reduction of P_{MAX} (Equation 4) and therefore linearity, the linearity of the PA is met due to the reduced power level. Figure 5 illustrates this approach for the case of a PCS CDMA power amplifier.

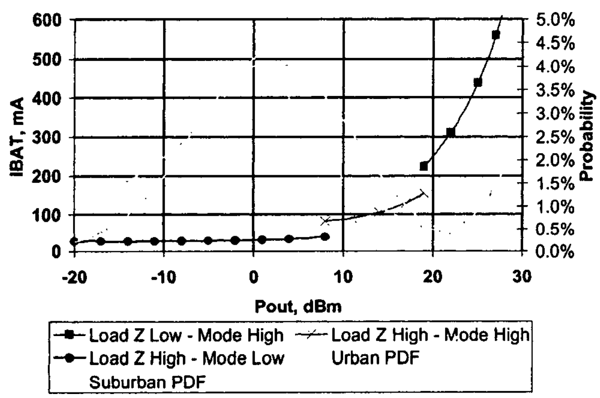

Fig. 5. 28dBm PCS Power Amplifier operating at 1880MHz, Vcc=3.4V

At the load switching power level of 19dBm, a 5 to 6 percent improvement in PAE can be achieved when the load is switched to a higher impedance while at the same time the quiescent current is reduced. When combined with an additional quiescent current reduction at 9dBm, this technique has been shown to provide an average current reduction of between 45 and 60 percent. Load switching capability is obtained at the expense of form factor and some increase in package and manufacturing cost. This expense, however, can be justified for challenging multi-mode PA applications.

IV. CONCLUSION

It has been shown for a CDMA or WCDMA power amplifier that by carefully controlling parameters such as quiescent current and operating voltage or load impedance to reduce the overall current consumption, the average efficiency of a mobile phone system is significantly increased (Table I). This increased efficiency translates directly into a decrease in average current consumption, leading to extended battery life between battery charges.

Techniques to control the quiescent current and operating voltage can be integrated into the power amplifier module or the system's PMIC, resulting in low cost, small form factor solutions. Quiescent current control can also be used in combination with load switching; the design is generally more challenging, and has some impact on PA module size and manufacturing cost.

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